

FEATURES

- 12-Bit, 20 MSPS Analog-to-Digital Converter
- Monolithic CMOS
- Internal Track-and-Hold
- Low Input Capacitance
- Low Power Dissipation: 76 mW
- 2.7 - 3.6 V Power Supply
- TTL-Compatible Outputs

APPLICATIONS

- CCD Imaging Cameras and Sensors
- Medical Imaging
- RF Communications
- Document and Film Scanners
- Electro-Optics
- Transient Signal Analysis
- Handheld Equipment

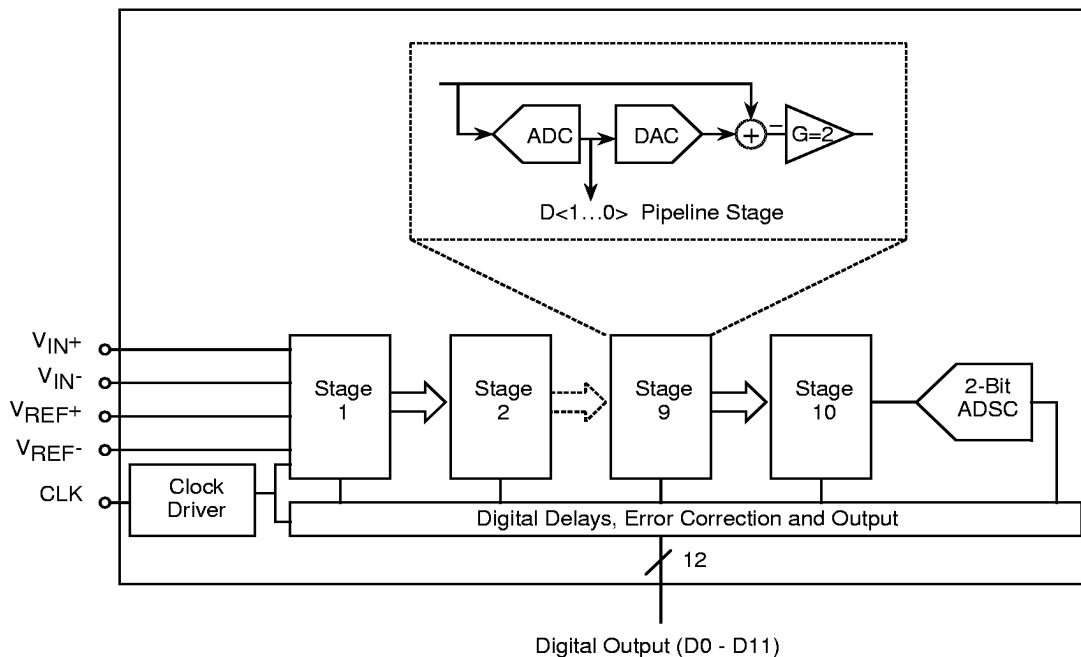
GENERAL DESCRIPTION

The SPT7935 12-Bit, 20 MSPS analog-to-digital converter has a pipelined converter architecture built in a monolithic CMOS process. It delivers excellent low noise performance with a typical power dissipation of only 76 mW. With low distortion and high dynamic range, this device offers the

performance needed for imaging, multimedia, telecommunications and instrumentation applications.

The SPT7935 is available in a 44-lead Thin Quad Flat Pack (TQFP) package in the commercial temperature range (0 to +70°C).

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)¹ 25 °C

Supply Voltages

V _{DD1}	-0.5V to +6 V
V _{DD2}	-0.5 V to +6 V

Temperature

Operating Temperature	0 to +70 °C
Storage Temperature	-65 to +125 °C

Input Voltages

Analog Input	-0.5 V to V _{DD1} +0.5 V
Digital Input	-0.5 V to V _{DD2} +0.5 V
V _{REF+}	-0.5 V to V _{DD1} +0.5 V
V _{REF-}	-0.5 V to V _{DD1} +0.5 V
CLK	-0.5 V to V _{DD2} +0.5 V

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7935			UNITS
			MIN	TYP	MAX	
DC Accuracy						
Resolution				12		Bits
Differential Linearity				±1.0		LSB
Integral Linearity				±3.0		LSB
Common Mode Rejection Ratio (CMRR)				TBD		
No Missing Codes				Guaranteed		
Analog Input						
Input Voltage Range				±1.0		V
Common Mode Input Voltage				1.5		V
Input Capacitance				1.2		pF
Input Bandwidth				TBD		MHz
Offset				TBD		LSB
Gain Error				TBD		LSB
Reference Voltages						
Reference Input Voltage Range (V _{REF+} - V _{REF-})			0.6	1.0	1.2	V
Negative Input Voltage (V _{REF-})				1.0		V
Positive Input Voltage (V _{REF+})				2.0		V
Common Mode Output Voltage			TBD	1.65	TBD	V
Switching Performance						
Maximum Conversion Rate			20			MHz
Pipeline Delay (See Timing Diagram)				7.5		Clocks
Aperture Delay Time				2		ns
Aperture Jitter Time				10		ps
Dynamic Performance						
Effective Number of Bits						
f _{IN} = 4.4995 MHz			9	9.3		Bits
f _{IN} = 18.991 MHz				8.7		Bits
Signal-To-Noise Ratio						
f _{IN} = 4.4995 MHz			60	62		dB
f _{IN} = 18.991 MHz				58		dB

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ELECTRICAL SPECIFICATIONS

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7935			UNITS
			MIN	TYP	MAX	
Dynamic Performance-Continued						
Differential Phase				TBD		
Differential Gain				TBD		
Signal-To-Noise and Distortion						
$f_{IN} = 4.4995$ MHz			56	58		dB
$f_{IN} = 18.991$ MHz				54		dB
Spurious Free Dynamic Range						
$f_{IN} = 4.4995$ MHz			60	65		dB
$f_{IN} = 18.991$ MHz				57		dB
Digital Inputs						
Logic 1 Voltage			80% V_{DD}			
Logic 0 Voltage					20% V_{DD}	
Maximum Input Current Low	$V_I = GND$				± 10	μA
Maximum Input Current High	$V_I = V_{DD}$				± 10	μA
Input Capacitance				1.2		pF
Digital Outputs						
Logic 1 Voltage	$I = 2$ mA		85% V_{DD}	90% V_{DD}		V
Logic 0 Voltage	$I = 2$ mA			0.2	0.4	V
Output Hold Time (t_H)				6		ns
Output DelayTime (t_D)				8		ns
Power Supply Requirements						
Supply Voltages						
V_{DD}			2.7	3.3	3.6	V
Supply Current						
I_{DD}				23		mA
Analog Power - Digital Power Pins			-0.2		+0.2	V
Digital Power - Output Driver Power			-0.2		+0.2	V
Power Dissipation				76		mW
Power Supply Rejection Ratio (PSRR)				TBD		dB

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions: All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

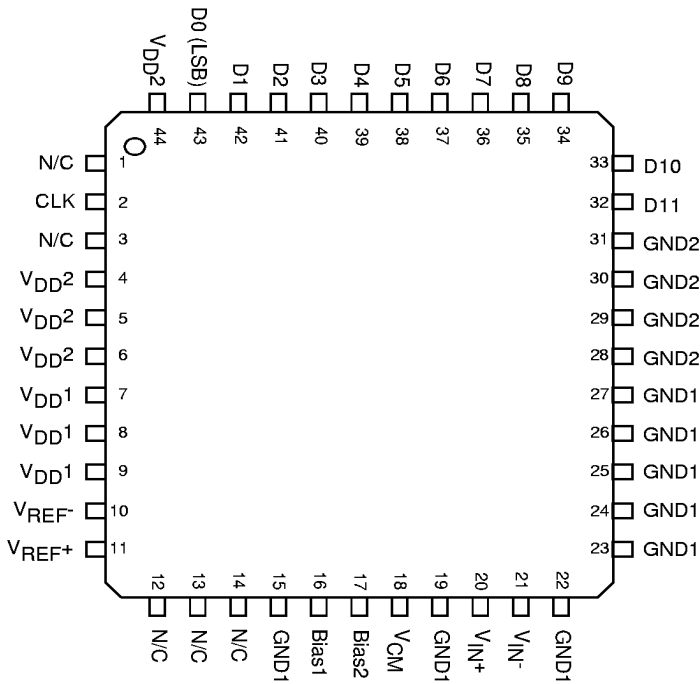
TEST LEVEL

I
II
III
IV
V
VI

TEST PROCEDURE

100% production tested at the specified temperature.
100% production tested at $T_A = +25$ °C, and sample tested at the specified temperatures.
QA sample tested only at the specified temperatures.
Parameter is guaranteed (but not tested) by design and characterization data.
Parameter is a typical value for information purposes only.
100% production tested at $T_A = +25$ °C. Parameter is guaranteed over specified temperature range.

PIN ASSIGNMENTS



PIN FUNCTIONS

Name	Function
V _{IN+} , V _{IN-}	Analog Inputs
V _{REF+} , V _{REF-}	External Reference Inputs
CLK	Input Clock
V _{CM}	Common Mode Output Voltage (1.65 V typ)
Bias1	Internal Bias current (85 μA typ)
Bias2	Internal Bias Current (7.5 μA typ)
D0 - D11	Digital Outputs (D0 = LSB)
GND1, GND2	Analog Grounds
V _{DD1} , V _{DD2}	+3.3 V Supplies
N/C	Not Connected

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE
SPT7935SCT	0 to +70 °C	44L TQFP

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Covered by Patent Numbers 5262779 and 5272481.

WARNING - LIFE SUPPORT APPLICATIONS POLICY - SPT products should not be used within Life Support Systems without the specific written consent of SPT. A Life Support System is a product or system intended to support or sustain life which, if it fails, can be reasonably expected to result in significant personal injury or death.

Signal Processing Technologies believes that ultrasonic cleaning of its products may damage the wire bonding, leading to device failure. It is therefore not recommended, and exposure of a device to such a process will void the product warranty.