SPT231

FAST SETTLING, WIDEBAND BUFFER/AMPLIFIER (A_V = ±1 to ±5)

General Description

The SPT231 Buffer/Amplifier is a wideband operational amplifier designed specifically for high-speed, low-gain applications. The SPT231 is based on a current feedback op amp topology-a unique design that both eliminates the gain-bandwidth tradeoff and permits unprecedented high-speed performance. (See table below.)

The SPT231 Buffer/Amplifier is the ideal design alternative to low precision open-loop buffers and oscillation-prone conventional op amps. The SPT231 offers precise gains from ±1.000 to ±5.000 and linearity that is a true 0.1%-even for demanding 50Ω loads. Open-loop buffers, on the other hand, offer a nominal gain of 0.95 ±0.03 and a linearity of only 3% for typical loads. A buffer's settling time may look impressive but it is usually specified at unrealistically large load resistances or when the effects of thermal tail are not included; the SPT231 Buffer/Amplifier settles to 0.05% in 15ns-while driving a 100Ω load.

Offsets and drifts, usually a low priority in conventional high-speed op amp designs, were not ignored in the SPT231; the input offset voltage is typically 1mV and input offset voltage drift is only 10µV/°C. The SPT231 is stable and oscillation-free across the entire gain range and since it's internally compensated, the user is saved the trouble of designing external compensation networks and having to "tweak" them in production. The absence of a gain-bandwidth tradeoff in the SPT231 allows performance to be predicted easily; the table below shows how the bandwidth is affected very little by changing the gain setting.

The SPT231 is constructed using thin film resistor/bipolar transistor technology, and is available in the following versions:

SPT231AIH	-25°C to +85°C	12-pin TO-8 can
SPT231AMH	-55°C to +125°C	12-pin TO-8 can, features burn-in and hermetic testing

Typical Performance

parameter	gain setting 1	2	5	−1	−2	−5	units
−3dB bandwidth	180	165	130	165	150	115	MHz
rise time (2V)	1.8	2.0	2.5	2.0	2.2	2.9	ns
slew rate	2.5	3	3	3	3	3	V/ns
settling time (to .1%)	12	12	12	12	12	15	ns

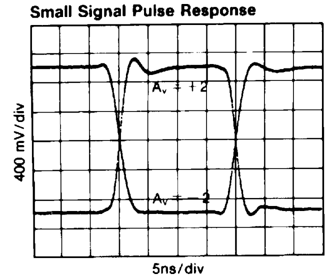
Features

- 165MHz closed-loop – -3dB bandwidth
- 15ns settling to 0.05%
- 1mV input offset voltage, 10µV/°C drift
- 100mA output current
- Excellent AC and DC linearity
- Direct replacement for CLC231

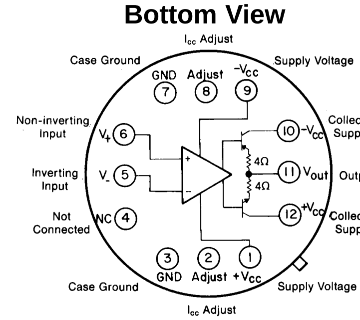
Applications

- Driving flash A/D converters
- Precision line driving
  (a gain of 2 cancels matched-line losses)
- DAC current-to-voltage conversion
- Low-power, high-speed applications
  (50mW @ ±5V)

Small Signal Pulse Response

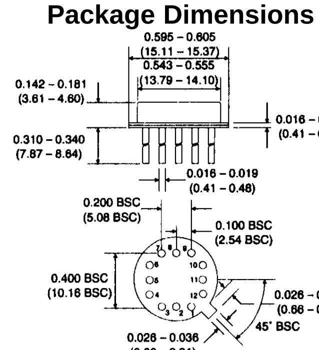


Bottom View



Pins 2 and 8 are used to adjust the supply current or to adjust the offset voltage (see text). These pins are normally left unconnected.

Package Dimensions



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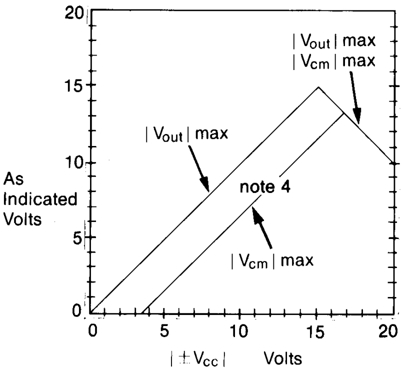
SPT231 Electrical Characteristics (A_V = +2, V_{CC} = ±15V, R_L = 100Ω, R_f = 250Ω; unless specified)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	SPT231AIH	+25°C	−55°C	+25°C	+125°C		
Ambient Temperature	SPT231AMH	+25°C	−25°C	+25°C	+85°C		
FREQUENCY DOMAIN PERFORMANCE							
† −3dB bandwidth note 2	$V_{out} \leq 2V_{pp}$	165	>145	>145	>120	MHz	SSBW
	$V_{out} \leq 10V_{pp}$	95	>80	>80	>60	MHz	FPBW
gain flatness note 2	$V_{out} \leq 2V_{pp}$						
† peaking	0.1 to 50MHz	0.1	<0.6	<0.3	<0.6	dB	GFPL
† peaking	>50MHz	0.1	<1.5	<0.3	<0.8	dB	GFPH
† rolloff	at 100MHz	0.4	<0.6	<0.6	<1.0	dB	GFR
group delay	to 100MHz	3.5±0.5	—	—	—	ns	GD
linear phase deviation	to 100MHz	0.5	<2	<2	<2	°	LPD
reverse isolation	to 100MHz						
non-inverting		53	>43	>43	>43	dB	RINI
inverting		36	>26	>26	>26	dB	RIIN
TIME DOMAIN PERFORMANCE							
rise and fall time	2V step	2	<2.4	<2.3	<2.7	ns	TRS
	10V step	5.0	<7.0	<6.5	<6.5	ns	TRL
settling time to .05%	5V step	15	—	—	—	ns	TS
to .1%	2.5V step	12	<22	<17	<22	ns	TSP
overshoot	5V step	5	<15	<10	<15	%	OS
slew rate (overdriven input)		3	>2.5	>2.5	>1.8	V/ns	SR
overload recovery	<1% error						
<50ns pulse, 200% overdrive		120	—	—	—	ns	OR
DISTORTION AND NOISE PERFORMANCE							
† 2nd harmonic distortion	0dBm, 20MHz	−55	<−47	<−47	<−47	dBc	HD2
† 3rd harmonic distortion	0dBm, 20MHz	−59	<−47	<−47	<−47	dBc	HD3
equivalent input noise							
noise floor	>5MHz	−153	<−150	<−150	<−150	dBm(1Hz)	SNF
integrated noise	5MHz to 200MHz	70	<100	<100	<100	µVrms	INV
STATIC, DC PERFORMANCE							
* input offset voltage		1	<4.0	<2.0	<4.5	mV	VIO
temperature coefficient		10	<25	<25	<25	µV/°C	DVIO
* input bias current	non-inverting	5	<29	<21	<31	µA	IBN
temperature coefficient		50	<125	<125	<125	nA/°C	DIBN
* input bias current	inverting	10	<31	<15	<35	µA	IBI
temperature coefficient		125	<200	<200	<200	nA/°C	DIBI
* power supply rejection ratio		50	>45	>45	>45	dB	PSRR
common mode rejection ratio		46	>40	>40	>40	dB	CMRR
* supply current	no load	18	<22	<22	<22	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input resistance		400	>100	>200	>400	kΩ	RIN
capacitance		1.3	<2.5	<2.5	<2.5	pF	CIN
output impedance	at 100MHz	5,37	—	—	—	Ω,nH	ZO
output voltage range	no load	±12	>±11	>±11	>±11	V	VO

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

Input and Common Mode Voltage Limits



supply voltage V_{cc}	±20V
output current	±100mA
thermal resistance (θ_{ca})	see thermal model
junction temperature	+175°C
operating temperature	AIH: −25°C to +85°C
	AMH: −55°C to +125°C
storage temperature	−65°C to +150°C
lead temperature (soldering 10s)	+300°C

note 1: * AIH, AMH 100% tested at 25°C.
† AMH 100% tested at +25°C & sample tested at -55°C & +125°C.
† AIH sample tested at +25°C.

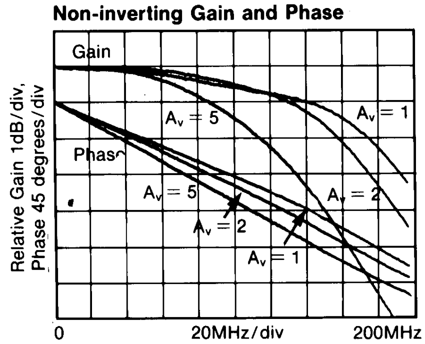
note 2: The output amplitude used in testing is $0.63V_{pp}$. Performance is guaranteed for conditions listed.

note 3: In the non-inverting configuration, care should be taken when choosing R_i, the input impedance setting resistor; bias currents of typically 5µA but as high as 24µA can create an input signal large enough to cause overload. It is therefore recommended that $R_i < (V_{cc}/A_v)/24\mu A$.

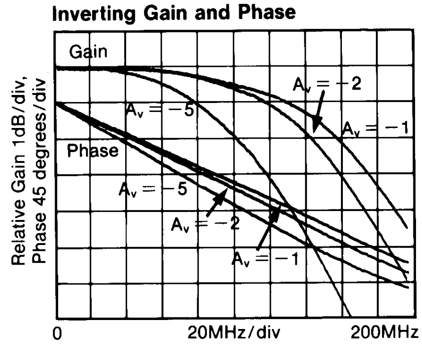
note 4: These ratings protect against damage to the input stage caused by saturation of either the input or output stages at lower supply voltages, and against exceeding transistor collector-emitter breakdown ratings at high supply voltages. V_{out}(max) is calculated by assuming no output saturation. Saturation is allowed to occur up to this calculated level of V_{out}. V_{cm} is defined as the voltage at the non-inverting input, pin 6.

SPT231 Typical Performance Characteristics (T_A = 25°, A_V = +2, V_{CC} = ±15V, R_L = 100Ω; unless specified)

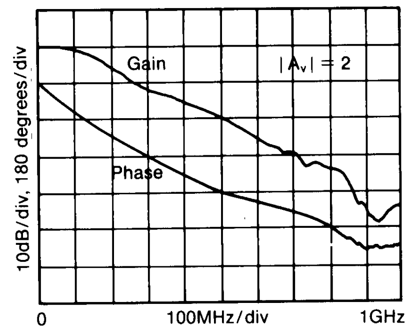
Non-inverting Gain and Phase



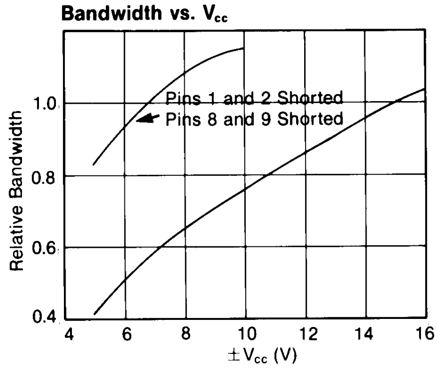
Inverting Gain and Phase



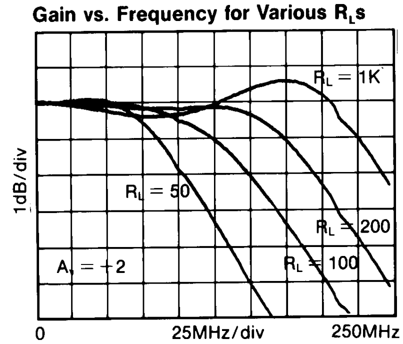
Broadband Gain and Phase



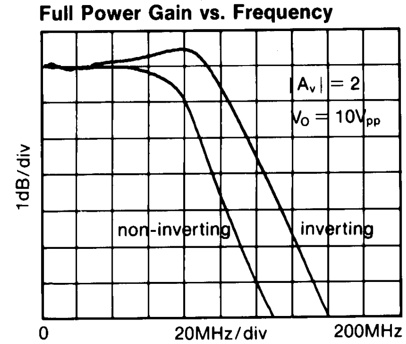
Bandwidth vs. V_{cc}



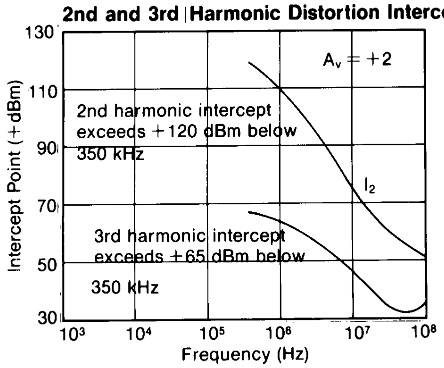
Gain vs. Frequency for Various R_Ls



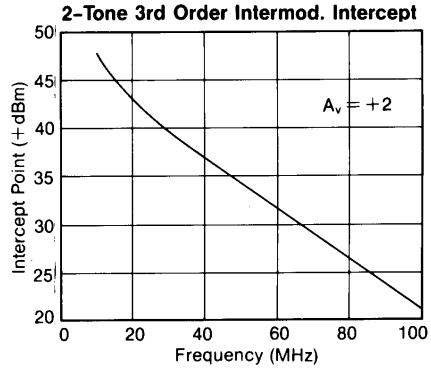
Full Power Gain vs. Frequency



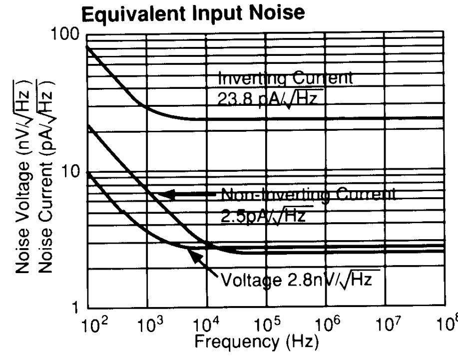
2nd and 3rd Harmonic Distortion Intercept



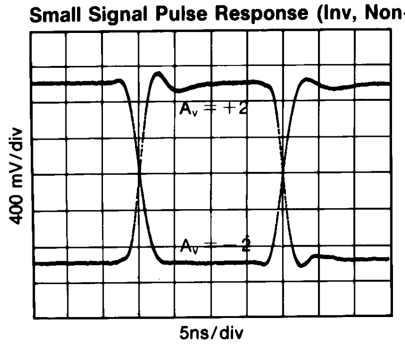
2-Tone 3rd Order Intermod. Intercept



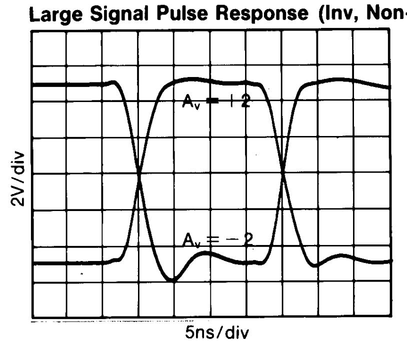
Equivalent Input Noise



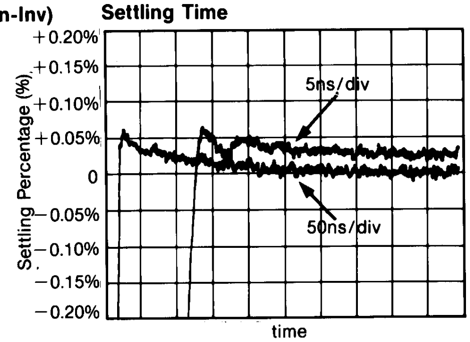
Small Signal Pulse Response (Inv, Non-Inv)



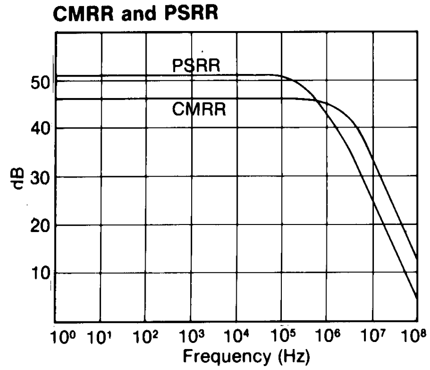
Large Signal Pulse Response (Inv, Non-Inv)



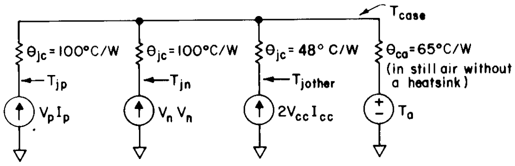
Settling Time



CMRR and PSRR



Thermal Model



$P_{circuit} = I_{cc}\,[(+V_{cc}) - (-V_{cc})]$ where I_{cc} = 16mA at ±15V

$P_{XXX} = [(\pm V_{cc}) - V_{out} - (I_{col})\,(R_{col} + 4)]\,(I_{col})$ (% duty cycle)

(For positive V_o and V_{cc}, this is the power in the npn output stage.)

(For negative V_o and V_{cc}, this is the power in the pnp output stage.)

$I_{col} = V_{out}/R_{load}$ or 4mA, whichever is greater. (Include feedback R in R_{load}.)

R_{col} is a resistor (33Ω recommended) between the xxx collector and $\pm V_{cc}$.

$T_{j\,(pnp)} = P_{pnp}\,(100 + \theta_{ca}) + (P_{cir} + P_{npn})\,\theta_{ca} + T_a$, similar for $T_{j\,(npn)}$.

$T_{j\,(cir)} = P_{cir}\,(48 + \theta_{ca}) + (P_{pnp} + P_{npn})\,\theta_{ca} + T_a$.

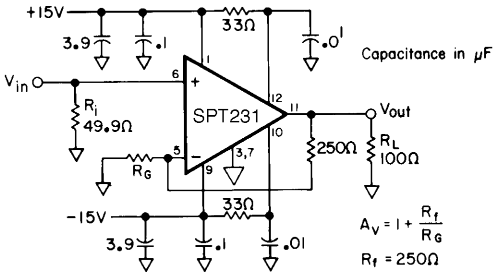


Figure 1: suggested non-inverting gain circuit

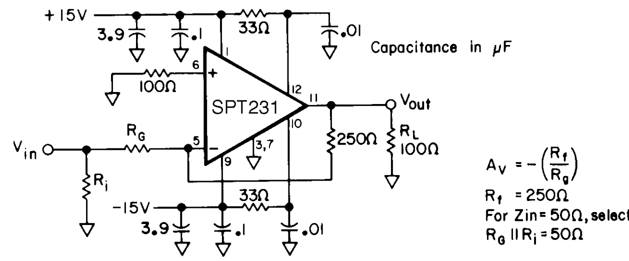


Figure 2: suggested inverting gain circuit

Operation

The SPT231 Buffer/Amplifier is based on the current feedback op amp topology, a design that uses current feedback instead of the usual voltage feedback.

The use of the SPT231 is basically the same as that of the conventional op amp (see the gain equations above). Since the device is designed specifically for low gain applications, the best performance is obtained when the circuit is used at gains between ±1 and ±5. Additionally, performance is optimum when a 250Ω feedback resistor is used.

Layout Considerations

To assure optimum performance the user should follow good layout practices which minimize the unwanted coupling of signals between nodes. During initial breadboarding of the circuit, use direct point to point wiring, keeping the lead lengths to less than .25". The use of solid, unbroken ground plane is helpful. Avoid wire-wrap type pc boards and methods. Sockets with small, short pin receptacles may be used with minimal performance degradation although their use is not recommended.

During pc board layout, keep all traces short and direct. The resistive body of R_g should be as close as possible to pin 5 to minimize capacitance at that point. For the same reason, remove ground plane from the vicinity of pins 5 and 6. In other areas, use as much ground plane as possible on one side of the board. It is especially important to provide a ground return path for current from the load resistor to the power supply bypass capacitors. Ceramic capacitors of .01 to .1μF (with short leads) should be less than .15 inches from pins 1 and 9. Larger tantalum capacitors should be placed within one inch of these pins. V_{cc} connections to pins 10 and 12 can be made directly from pins 9 and 1, but better supply rejection and settling time are obtained if they are separately bypassed as in figures 1 and 2. To prevent signal distortion caused by reflections from impedance mismatches, use terminated microstrip or coaxial cable when the signal must traverse more than a few inches.

Since the pc board forms such an important part of the circuit, much time can be saved if prototype boards of any high frequency sections are built and tested early in the design phase. Evaluation boards designed for either inverting or non-inverting gains are available.

Thermal Considerations

At high ambient temperatures or large internal power dissipations, heat sinking is required to maintain acceptable junction temperatures. Use the thermal model on the previous page to determine junction temperatures. Many styles of heat sinks are available for TO-8 packages; the Thermalloy 2240 and 2268 are good examples. Some heat sinks are the radial fin type which cover the pc board and may interfere with external components. An excellent solution to this problem is to use surface mounted resistors and capacitors. They have a very low profile and actually improve high frequency performance. For use of these heat sinks with conventional components, a .1" high spacer can be inserted under the TO-8 package to allow sufficient clearance.

Low V_{cc} Operation: Supply Current Adjustment

The SPT231 is designed to operate on supplies as low as ±5V. In order to improve full bandwidth at reduced supply voltages, the supply current (I_{cc}) must be increased. The plot of Bandwidth vs V_{cc} shows the effect of shorting pins 1 and 2 and pins 8 and 9; this will increase both bandwidth and supply current. Care should be taken to not exceed the maximum junction temperatures; for this reason this technique should not be used with supplies exceeding ±10V. For intermediate values of V_{cc}, external resistors between pins 1 and 2 and pins 8 and 9 can be used.

Offset Voltage Adjustment

If trimming of the input offset voltage ($V_{os} = V_{ni} - V_{in}$) is desired, a resistor value of 10kΩ to 1MΩ placed between pins 8 and 9 will cause V_{os} to become more negative by 8mV to 0.2mV respectively. Similarly, a resistor placed between pins 1 and 2 will cause V_{os} to become more positive.

Distortion and Noise

The graphs of intercept point, I_2 and I_3, versus frequency on the preceding page make it easy to predict the distortion at any frequency given the output voltage of the SPT231. First, convert the output voltage (V_O) to $V_{RMS} = (V_{pp}/2\sqrt{2})$ and then to $P = [(10\log_{10}(20V_{RMS}^2)]$ to get the power output in dBm. At the frequency of interest, its 2nd harmonic will be $S_2 = (I_2 - P)$dB below the level of P. Its third harmonic will be $S_3 = 2(I_3 - P)$dB below P, as will the two-tone third order intermodulation products. These approximations are useful for $P < -1$dB compression levels.

Approximate noise figure can be determined for the SPT231 using the equivalent input noise graph on the preceding page. The following equation can be used to determine noise figure (F) in dB.

$$F = 10\log\left[1 + \frac{v_n^2 + \dfrac{i_n^2\,R_F^2}{A_v^2}}{4kTR_s\Delta f}\right]$$

Where v_n is the rms noise voltage and i_n is the rms noise current. Beyond the breakpoint of the curves (i.e., where they are flat), broadband noise figure equals spot noise figure, so Δf should equal one (1) and v_n and i_n should be read directly off the graph. Below the breakpoint, the noise must be integrated and Δf set to the appropriate bandwidth.