## FEATURES

- 10-Bit Triple Video Digital-to-Analog Converter
- Output Full-Scale Voltage 0.5 to $2.0 \mathrm{Vp}-\mathrm{p}$
- 36 MWPS Operation (typ)
- Low Power: 280 mW (1 Vp-p Output)
- 5 V Monolithic CMOS
- 52-pin QFP Package ( $10 \mathrm{~mm} \times 10 \mathrm{~mm}, 0.65 \mathrm{~mm}$ pitch)


## APPLICATIONS

- Desktop Video Processing
- CCIR-601 Video Signal Processing
- RGB Color Monitors
- Image Processing
- Direct Digital Synthesis


## GENERAL DESCRIPTION

The SPT5230 is a 10 -bit, 36 MWPS triple video digital-toanalog converter specifically designed for high performance, high resolution color graphics monitor applications and video processing applications. A single external resistor controls
the full-scale output current. The differential linearity errors of the DACs are guaranteed to be a maximum of $\pm 1.0 \mathrm{LSB}$ over the full temperature range. The device is available in a 52lead QFP package over the commercial temperature range.

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)1

Supply Voltages<br>$A V_{D D}$ (measured to $A V_{S S}$ )<br>$\qquad$<br>\section*{Input Voltage}<br>Clock and Data<br>$\qquad$ $A V_{S s}$ to $A V_{D D}$

## Output Current

Iout 0 to 14 mA

Temperature
Operating, ambient ....................................... 0 to $+70^{\circ} \mathrm{C}$ Storage ................................................ -55 to $+125^{\circ} \mathrm{C}$

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

## ELECTRICAL SPECIFICATIONS

$\mathrm{f}_{\mathrm{CLK}}=27$ MWPS, $\mathrm{AV}_{\mathrm{DD}}=5.0 \mathrm{~V}$, Output Pull-Up Load $=75 \Omega, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{AV}$ SS $=0.0 \mathrm{~V}$

| PARAMETERS | TEST <br> CONDITIONS | TEST <br> LEVEL | MIN | TYP | MAX |
| :--- | :--- | :--- | :--- | :--- | :--- | UNITS

1 Full-scale settling time to within $\pm 2 \%$ of full scale.

## TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

## TEST LEVEL TEST PROCEDURE

III QA sample tested only at the specified temperatures.
IV Parameter is guaranteed (but not tested) by design and characterization data.
Parameter is a typical value for information purposes only.
$100 \%$ production tested at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$. Parameter is guaranteed over specified temperature range.

## INTERFACE CONSIDERATIONS

Figure 4 shows a typical interface circuit of the SPT5230 in normal circuit operation.

## SUPPLY AND GROUND CONSIDERATIONS

Fairchild suggests that all power supply pins (AVDD) be tied together and decoupled using a $0.1 \mu \mathrm{~F}$ ceramic capacitor in parallel with a $10 \mu \mathrm{~F}$ tantalum capacitor.

## EXTERNAL REFERENCE VOLTAGE (VREF1)

$\mathrm{A}+3 \mathrm{~V}( \pm 10 \%)$ voltage reference should be externally generated for the $\mathrm{V}_{\text {REF1 }}$ pin using the simple voltage divider shown in figure 4 . Connect a $0.1 \mu \mathrm{~F}$ bypass capacitor between $\mathrm{V}_{\text {REF1 }}$ and AV SS as close to the pin as possible.

## EXTERNAL REFERENCE VOLTAGE (VREF2)

$V_{\text {REF2 }}$ needs to be externally connected to $A V_{D D}$ through a $1.2 \mathrm{k} \Omega(5 \%)$ resistor. Connect a $0.1 \mu \mathrm{~F}$ bypass capacitor between $\mathrm{V}_{\text {REF2 }}$ and $\mathrm{AV}_{\mathrm{SS}}$ as close to the pin as possible.

## CONTROL VOLTAGE DECOUPLING (VCS1)

This is a decoupling pin for the control voltage internal circuitry. An external $0.1 \mu \mathrm{~F}$ capacitor should be connected between $\mathrm{V}_{\mathrm{CS} 1}$ and AV SS as close to the pin as possible.

## FULL-SCALE ADJUST CONTROL ( $\mathbf{V}_{\text {CS2 }}$ )

$\mathrm{V}_{\mathrm{CS} 2}$ is an external control voltage input that controls the peak-to-peak full scale output voltage. This is the only external voltage that has direct control over the SPT5230 output voltage. The voltage output swings between $\mathrm{AV}_{\mathrm{DD}}(+5 \mathrm{~V})$ and a value controlled by $\mathrm{V}_{\mathrm{CS}}$.

Assuming that an output load resistor of $75 \Omega$ is connected between the output and $A V_{D D}$, figure 2 shows what the output voltage will be for the digital inputs all equal to logic 0 , as $\mathrm{V}_{\text {CS2 }}$ is varied from 2 V to 4 V . Figure 3 shows the peak-to-peak output voltage versus $V_{C S 2}$ and table I shows an example in which $\mathrm{V}_{\mathrm{CS} 2}$ is equal to 2.1 V .

## CURRENT OUTPUTS

Each red, green and blue current output should have a load resistor connected to $A V_{D D}$. The resistors are typically $75 \Omega$ and should be kept in the $72 \Omega$ to $85 \Omega$ range. The outputs should drive a high impedance load such as a voltage follower.

## OUTPUT LEVEL SHIFTING CIRCUIT

The SPT5230 voltage output will swing from +3.0 V to +4.99 V for $\mathrm{V}_{\mathrm{CS} 2}=2.1 \mathrm{~V}$ as shown in table I . If level shifting of the output is desired, Fairchild recommends use of the circuit shown in figure 5. The desired -FS voltage is fed into the collector of the emitter to achieve the desired level shift. (Note the phase inversion that will occur due to the common emitter.) Choose any appropriate video op amp with adequate power supply head room.

## Table I- Binary Codes <br> $1 \mathrm{LSB}=1.953 \mathrm{mV}, \mathrm{VCS} 2 \approx 2.1 \mathrm{~V}$



Figure 1 - Timing Diagram


Figure 2 - Output Voltage with All Digital Inputs = Ø versus VCS2


NOTE: For Digital Inputs $=$ All 1, Output Voltage $=+4.998047 \mathrm{~V}$.

Figure 3 - Output Voltage (Vp-p) versus Vcs2


Figure 4 - Typical Interface Circuit


Figure 5 - Recommended Output Level Shifting Circuit


## PACKAGE OUTLINE

## 52-Lead QFP



## PIN ASSIGNMENTS



## PIN FUNCTIONS

Name Function

| Rout | Red Analog Current Output |
| :---: | :---: |
| Gout | Green Analog Current Output |
| BOUT | Blue Analog Current Output |
| R0-R9 | Red Data Inputs |
| G0-G9 | Green Data Inputs |
| B0-B9 | Blue Data Inputs |
| CLKR | Red Clock Input |
| CLKG | Green Clock Input |
| CLKB | Blue Clock Input |
| VREF1 | Voltage Reference Input 1 (A $0.1 \mu \mathrm{~F}$ ceramic capacitor should be used.) |
| VREF2 | Voltage Reference Input 2 <br> (A $0.1 \mu \mathrm{~F}$ ceramic capacitor should be used.) |
| VCS1 | Control Voltage Decoupling (A $0.1 \mu \mathrm{~F}$ ceramic capacitor should be used.) |
| $\mathrm{V}_{\text {CS2 }}$ | Full-Scale Adjust Control Voltage (A $0.1 \mu \mathrm{~F}$ ceramic capacitor should be used.) |
| AVSS | Analog Ground |
| AVDD | Analog Power Supply Voltage |
| N/C | No Connection |

## ORDERING INFORMATION

| PART NUMBER | TEMPERATURE RANGE | PACKAGE |
| :--- | :---: | :---: |
| SPT5230SCT | 0 to $+70^{\circ} \mathrm{C}$ | 52 L QFP |

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